SYSTEMATIC DESIGN OF DISSIPATIVE AND REGENERATIVE SNUBBERS

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ABSTRACT

Current commutation between diodes and switches is possible in hard-switching power-stages over a wide di/dt range, (10-1000+ A/µs) with modern power-devices and hardware practice. Yet, a definitive procedure does not exist for setting di/dt at diode reverse-recovery. Diode turn-off performance is therefore examined, using IGBT's to switch diode-current, to establish if an optimal di/dt exists which minimizes energy-loss associated with diode recovery, when simple snubber-inductance reset circuits are used. Destructive parasitic-oscillation, induced in inverse-parallel IGBT's across reverse recovering freewheel-diodes in IGBT modules, were obtained during experimentation. The origin and cure are presented.

INTRODUCTION

Device manufacturers and users are promoting the view that hard-switching power-stages, using the latest power devices, are best operated with virtually no snubbers [1], ie. with little current or voltage transient control other than 'active' snubbing or clamping through switch-drive control, or by device avalanche, or by tailoring device-response (soft-recovery diodes) at turn-off; and devices are being examined to quantify snubberless operating regions [2,3]. However, while this may be desirable from a manufacturer's standpoint, because snubberless designs are generally less forgiving of device-type variation, from a user's point-of-view it is less so, as it represents the removal rather than gradual lowering of a safety-net. Device switching-transitions are heavily dependent upon a host of device, component and hardware characteristics, subject to production-spread and voltage, current and temperature variation. Therefore, with no snubbing or clamping, bracketing emi-emission and power-stage reliability on a sampling basis, must be compounded by loss of consistency in device-stress and magnitude and frequency of voltage and current overshoot and ringing at transitions. With modern devices, snubbers are used more to clamp turn-off voltage overshoot due to energy transfer between series-inductance and effective device-capacitance at turn-off [$V_{os}=I_{off}\sqrt{(L_{series}/C_{op})}$], and to clamp turn-on current due to energy transfer between freewheel-diode (reverse-recovery) capacitance and series-inductance [$I_{os}=E_{dc}\sqrt{(C_{diode}/L_{series})}$]. Conflicting requirements, therefore, exist for minimal current and voltage overshoot; and it is worth noting that transient magnitude and damping (with RC-snubber $\zeta=R/2\sqrt{C/L}$) are set by the ratio of effective energy-storage components rather than their absolute value, resulting in such paradoxes as transient amplitude and damping may worsen, and noise amplitude coupled into control circuits may increase, when faster devices and tighter hardware-layout are used: reduced circuit-geometry increases parasitic resonant-circuit frequency (30-500 MHz later shown) and initial di/dt and dv/dt; and, so, reduced overlapping conductor loops and plates are required for the same degree of electromagnetic or electro-static coupling. The advantage of smaller resonant-circuits, of course, is reduced energy-loss in their damping, but the small RC-snubbers required to realize it may be overlooked if their is a headlong rush to be snubberless, or to have snubberless devices. Small RC-snubbers, although difficult to design [4], attenuate switching-noise at source, reducing filtering and screening below that required by a snubberless design. Also, apart from greater noise generation, and reduced flexibility in accommodating modification, upgrading and device variation, snubberless power-stages using active-snubbing by gate or drive control, are fundamentally less thermally efficient than snubbered power-stages using the best forms of passive-component snubbing [1]. However, whether active or passive snubbing is used, a procedure for optimizing freewheel-diode reverse-recovery di/dt for minimal power-loss does not seem to exist. An examination of the energy-loss associated with diode-recovery under various switching conditions is, therefore, presented.

COMPARISON OF ACTIVE AND PASSIVE SNUBBING

Idealized waveforms for active and passive turn-on snubbing are given in fig.1. In fig.1A the gate-drive is assumed to produce the same turn-on di/dt and peak diode reverse-recovery current as the series-snubber inductance of fig.1B. Instantaneous-power plots show that passive-snubber energy is transferred from Lseries to the load and the remainder dissipated in voltage clamps, whereas in active-snubbing, no energy transfer occurs and greater energy-loss is concentrated in the switch at turn-on. Wactive/Wpassive (fig.2) gives a maximum of 2 when Irm=Io. In practice, stray-inductance lowers switch-voltage in active-snubber circuits, reducing switch energy-loss (fig.9), and dynamic-saturation-type effects raise switch-voltage, increasing energy-loss (fig.11 &12) in passive-snubber circuits at turn-on.

Modern medium-current (10-100 A) power devices are quite tolerant of high turn-off dv/dt, and it is usually only necessary to clamp voltage transients to uphold voltage or repetitive-avalanche ratings, particularly with parallel-connected devices or multiple-dice switches where energy-loss would be concentrated in the first device to breakover. Like current-transient control at turn-on, voltage transient at turn-off is controllable with active or passive snubbing or clamping. A more complete active/passive comparison is given in [1]. Here, fig.3 gives energy-loss for true and artificial device-avalanche, defined to constitute active snubbing or clamping, and for passive snubbing with an RC-snubber or soft voltage-clamp. With active-clamping or RC-snubbing a multiple of the trapped energy, $L_{series}I_o^2/2$, is dissipated [$(1+2/X^2)$ or $(1+E_{dc}/V_{os})$]; whereas the best passive clamp, soft voltage-clamp, dissipates trapped-energy without multiplication, and also clamps at the prevailing dc-rail value and gives relatively constant Lseries and Cclamp reset-time, irrespective of switched current or dc-rail voltage (fig.5C & 6). With idealized turn-on and turn-off waveforms and usual current or voltage modulation, it is apparent that passive-snubbing is more efficient. In practice, active and passive snubbing take place together to some extent, because, in either, Lseries

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or switch-voltage is not zero; and it is less obvious that passive snubbing is still fundamentally more efficient. However this can be shown.

Irm, di/dt, Vswitch and switch energy-loss, Wswon, were measured at IGBT (Toshiba MG25H2YS1) turn-on, with Io between 6 and 31A freewheeling in a series connected IGBT-module diode, for both active and passive snubbing. From measured Irm, di/dt, Vswitch and eqn.4 and 6 (appendix), total active and passive energy-loss is obtained (fig.17). It is evident that an energy-loss saving of up to 40% is obtained with passive snubbing over the 25A current range; and although measured Wswon is significantly higher (fig.15 & 16) than that calculated from measured parameters, the true difference between active and passive snubbing energy-loss is likely to be higher than shown in fig.17, because estimation of active energy-loss is particularly low. The reason is the greater current non-linearity, varying switch-voltage and sustained current Irm-peak and switch voltage-fall obtained with active snubbing.

RESETTING SERIES-SNUBBERS

Optimization of soft voltage-clamps (fig.7A) to rapidly reset Lseries is important at high chopping-frequency. Clamp-capacitor voltage, and inductor and resistor current waveforms (fig.5C & 6) show the relatively constant Lseries and Cclamp reset times and well controlled response of optimized clamps, at 150V, 250V and 600V for 10 to 100A. Fig.5B gives responses for clamp resistance either side of the optimum (2.2Ω), to show that either Cclamp or Lseries reset times are extended. Also, slight circuit overdamping prevents the oscillation seen at clamp-diode recovery with the fastest current reset, but slowest voltage reset, when R=4.7Ω. Soft voltage-clamp optimization is performed on the curves of fig.4C and 4D [5]. From the normalized overshoot above the dc-rail, Vcpn, and capacitor reset-time, trvn, graph (fig.4C), trvn is seen to pass through a minimum as Vcpn decreases. Normalized Lseries reset time, trvn, increases rapidly above this optimum (fig.4D). The optimum trvn is evident from computed waveforms (fig.4A & B). Minimal total reset-time is obtained with trin (fig.4D) set above the minimum. At high-current a small parallel-connected RC-snubber is required across switch/diode pairs to limit fast initial voltage-transients on clamp parasitic series-inductance (fig.5A). Waveforms fig.5D give diode and switch voltage for a bridge-leg (fig.7B), where switch clamps double as diode clamps. With integrated switch and diode pairs (e.g. IGBT and MOSFET bridge-leg modules) fig.7B is unusable, but alternative circuits do exist (fig.7C & D). Fig.7D has significant disadvantages. Devices are clamped by three diodes in series with the clamp capacitor and observation of device-voltage is made difficult by inductor voltage. Series-diode number is reduced to two in fig.7C, which proves adequate when small RC-snubbers are used to suppress fast initial transients on clamp inductance [4]. A more accessible equivalent circuit is given for fig.7D (fig.7E). Direct connection of clamps across inverse-parallel device pairs (fig.7B) provides the hardest initial clamping with fast switches. Having to overcome three diode forward-recovery and parasitic inductance effects (fig.7D) is avoided, and observation of device voltage is uncomplicated. The same argument applies to regenerative snubbers, fig.8A and fig.8B, and, yet, fig.8A is more commonly examined, [6] and [7], which has more disadvantages than fig.7D because stray inductance is not clamped as part of the series-snubbers. Hence greater RCD-snubber capacity is required.

This section is mainly about turn-off passive snubbers or clamps to show that resetting Lseries, without trapped energy multiplication, is straight-forward, practically. Most soft voltage-clamp circuits are reduceable to the simplest configuration (fig.7A) for design, the minutiae of which is more fully covered in [1] [4] and [5]. Generally clamp-development effort is related to the speed of response and capacity required, with fast high-capacity clamps being more demanding. Also, re-iterating introductory remarks: design is complicated by conflict between optimum turn-on and turn-off conditions. Minimizing Lseries facilitates switch turn-off clamping, but complicates diode clamping through potentially higher more abrupt Irm. Turn-on and turn-off influences are now considered in the optimization of Lseries to minimise total energy-loss.

NON-LINEAR SERIES SNUBBING

Good soft-voltage clamp efficiency arises from clamping and resetting to the dc-rail voltage, rather than 0V. The turn-on corollary of this for minimal reset-loss, is that series snubbing is only required after switch current exceeds freewheeling load-current when diode recovery begins (fig.1F). Energy-loss associated with four current-rise types, relative to that of linear-inductor series-snubbing, is given in fig.1. For saturable-reactor type rises (fig.1D & E) W/Wb increases from L1/L2 at K=0 (K=Irm/Io) to 1 at higher K. Scope for reduction in energy-loss is, therefore, determinable by letting K=0; and is confirmed by W/Wb plots (fig.14). The ideal current-rise, a current dual of the soft voltage-clamp voltage response at turn-off (fig.1F), is equivalent to fig.1E with L1/L2=0 and gives the lowest curve in fig.14. For L1/L2>0 (fig.1E) a family of higher curves is produced showing reduced energy-loss saving. A notable advantage of fig.1E and 1F type rises, over that produced by saturable reactors in bridge-legs (fig.1D), is reduced fall-off in energy-loss reduction with increasing K (fig.14). Energy-loss reduction for fig.1D falls off sharply as Irm approaches Io and the L1 region is reduced. Saturable reactors, also, by lowering load-current di/dt rather than just diode di/dt significantly reduce current-loop bandwidth when Io<=Irm(worst-case), which exacebates low-current distortion and current-loop stability. A true current dual to the soft voltage-clamp would eliminate these problems. Most current duals to voltage snubbers (fig.13) are well known. Although, with constant load current, the RL-snubber (fig.13B) gives the required current rise, after diode recovery Lseries takes up Io and no energy-loss saving results. The principle of a voltage-clamp dual is illustrated by fig.13C which is only valid for constant or slowly changing load-current, Io, because duality requires that Io is kept circulating in a higher than normal snubber inductor, L2, and rapidly commutated to and from the switch at turn-on and turn-off. Diode-recovery is controlled by L2. In principle, L1 and R are only required to prevent Irm staircasing in L2. Energy-loss is related to L1, although L2 sets diode recovery di/dt. In practice, Dc is as imperfect as Dfw, making realization difficult. Saturable reactors, therefore, seem the only feasible method of synthesizing non-linear current-rise, apart from using the current limiting property of switches, ie. returning to active-snubbing with its greater loss than linear inductance. Greater flexibility, more consistent turn-on stress, and ease of design and testing make a strong case for sticking with linear inductors, by maximising their utilization.

LINEAR SERIES SNUBBERS

With linear series snubbers, Lseries total reset energy-loss is given by, eqn.1, if load current, Io, is assumed constant and switch voltage is assumed negligible.

$$W_{tp} = \frac{1}{2} \text{Lseries } (I_{rm}^{2} + I_{o}^{2}) \qquad (1)$$

At low di/dt Wtp is predominantly due to Io at turn-off. As di/dt is increased, by reducing Lseries, Io associated loss reduction is counteracted by increasing Irm associated loss, and Wtp passes through a minimum. The minimum for Siemens BYP103 diode (fig.18) at 100°C is near 600 A/µs, but faster lower voltage diodes have minima at higher di/dt. A minimum is not obtained with active snubbing (fig.18) in the examined di/dt range, when Lseries=0 and Wta is given by eqn.2.

$$\text{Wta} = \frac{1}{2} E_{dc} / \frac{di}{dt} (I_{rm} + I_{o})^{2} \qquad (2)$$

In, practice, ideal active and passive snubbing conditions are virtually impossible to obtain and Lseries>0 and Vswitch>0 apply in both. Wta and Wtp (eqn.4 & 6) give the increased energy-loss shown in fig.19; where maximum Vswitch, VA (scale in fig.20), and Lseries-range for passive and active snubbing, respectively, are based on measurements. Pronounced minima are now obtained in both sets of curves. With active snubbing, energy-loss at turn-on is reduced, but Lseries avalanches the freewheel-diode and switch, when either turns off while conducting Irm or Io; and trapped energy undergoes high multiplication (fig.3) during reset. No further examination is made of active snubbing because of the distinct energy-loss advantage of passive snubbing.

Considering additional sources of energy-loss imposed by high di/dt lowers optimal di/dt even further. Small RC-snubbers are essential to compensate for voltage-clamp inductance otherwise severe ringing ensues (fig.11 & 12). In bridge-legs two are required which are not significantly assistant, in practice. Therefore, RC-snubber loss (fig.3) is doubled at each switching instant, and Wtp increases from eqn.6 to eqn.12. With Wpa becoming more Irm dependent minima are more pronounced (fig.20) and Vswitch has less influence on optimum di/dt. Optimum di/dt depends more on diode performance alone. With Vswitch=0, Wtp (eqn.12) is plotted using BY103 Irm data (fig.18) under various operating conditions. With Tj=100°C and Lclamp=50nH, Wtp variation with RC-snubber or overshoot is given (fig.21). Similarly, energy-loss variation with Lclamp and junction temperature variation is obtained (fig.22 & 23). With any parameter variation, the common trend is that more consistent performance is attainable at low di/dt (ie. contours are closer) and a significant energy-loss advantage results from operating near optimum di/dt (ie. below 400A/µs) rather than at the highest possible value. Similar graphs for 400V and 600V diodes give minima centred on higher di/dt. It is not the objective here to determine optimum di/dt precisely, but to show that one exists and the factors influencing it. Optimum di/dt will vary between diodes of similar rating, as seen by Wtp curves (fig.25) for four 30A, 1000-1200V diodes, for which Irm was measured (fig.24) under the same operating conditions. Diode switching-loss was, also, measured by integrating turn-off crossover waveforms (fig.25). The relatively flat curves do not influence optimum di/dt significantly.

With slower soft-recovery diodes turn-off (fig.27A & C), as with IGBT turn-off (fig.28), RC-snubbers seem unnecessary with voltage-clamps. However, it is difficult to know if a good device will have a turn-off like fig.27B, where initial di/dt approaches that of an abrupt diode. It would, also, be useful to know how consistent is the tendency for less abrupt current-fall at higher If (fig.26A,26C & 27D), which also alleviates RC-snubber requirment.

STIFF DRIVE CIRCUITS

The characteristics of 1000 V, 25 A IXYS and Toshiba integrated IGBT-module diodes were examined. Both devices could be operated at di/dt up to 300A/µs. However, above 300A/µs IXYS device failure occurred. Common-mode parasitic oscillation [8] was found to be the cause (fig.30B). Although Toshiba device testing was possible above 1000A/µs, with only a base-collector short-circuit holding off the upper IGBT, parasitic oscillation was also found to occur, but at a much higher frequency (565MHz). Parasitic oscillation of the upper device is noticeable in the lower device current (fig.29C & D) when series inductance is low, but may be overlooked on a slow oscilloscope (fig.29A & B). As with MOSFET's the cure is to add or increase gate-resistance (fig.29D). IXYS device parasitic oscillation occurs at lower frequency (fig.30B) but can destroy devices. The impact of adding gate resistance is evident in the currents and voltages of the upper device (fig.30 & 31C). A negative gate-bias alone on upper devices is not a sufficient cure (fig.31). Although gate-current resonance is modified, it is not positively damped. In most drives both gate-resistance and reverse gate-bias are used. The poorer waveforms (fig.32A & B)) than with resistance alone, are likely due to common-mode transient voltage effects in the bias power supply: using Rg alone (fig30C) does not involve bias power-supply connection. Waveforms produced by inadequate drive common-mode rejection (fig.32C & D) on high-side switch drives are included to show the difference between this and parasitic oscillation effects. While fig.10C shows that Rg should be minimised to reduce turn-off power-loss, it is necessary to provide good parasitic-oscillation damping, and Rg, not negative gate-bias, positively cures the problem.

CONCLUSIONS

The objective had been to dispel some commonly held beliefs about the best way of operating switching devices which appear contrary to the facts. It has been shown that snubberless power-stage operation, where active snubbing must be used to control switching transitions, is fundamentally less efficient than the best passive snubbing methods, very high di/dt operation of diodes is undesirable and very stiff power-switch drive circuits may lead to device failure in snubberless power stages.

APPENDIX

Equations for energy-loss used for fig.15, 16 & 17.
Lseries=snubber or stray inductance, or both added

Ls	= Lseries
Io	= load-current at switch turn-off or turn-on
Irm	= peak reverse-recovery diode current
Va	= switch or diode avalanche-voltage (1000V)
Vos	= Va - Edc
Vswitch	= switch voltage at turn-on during di/dt
Wswon	= switch energy-loss at turn-on during di/dt
Wswoff	= switch energy-loss at turn-off with avalanche
Wdoff	= diode energy-loss at peak of diode recovery during avalanche
Wdcl	= energy-loss in diode soft voltage-clamp
Wswcl	= energy-loss in switch soft voltage-clamp
Wta	= total energy-loss during one switch-cycle with active snubbing
Wtp	= total energy-loss during one switch-cycle with passive snubbing

$$Wta = [Wswon]+[Wdoff+Wswoff] \quad (3)$$

$$Wta = \left(\frac{Edc}{di/dt} - Ls\right)\frac{(Irm+Io)^2}{2} + \left(1+\frac{Edc}{Vos}\right)\frac{(Irm^2+Io^2)}{2}Ls \quad (4)$$

$$Wtp = [Wswon]+[Wdcl+ Wswcl] \quad (5)$$

$$Wtp = \frac{Vswitch}{di/dt}\frac{(Irm+Io)^2}{2} + \frac{(Irm^2+Io^2)}{2}Ls \quad (6)$$

Energy-loss associated with RC-snubber operation.
Energy-loss at switch turn-off.

$$Woff \approx C\,Edc^2/2+LsIo^2/2 \quad (7)$$

Energy-loss at switch turn-on. $Won= C\,Edc^2/2$ (8)

Total energy loss $Wrc \approx 2\,C\,Edc^2/2 + L\,Io^2/2$ (9)

If $X = (Io/Edc)\sqrt{(Ls/C)}$ then $Edc^2= (I/X^2)Ls/C$ (10)

Therefore $Wrc \approx (1+2/x^2)\,Ls\,Io^2/2$ (11)

Energy-loss of any voltage clamp can be put in the form of energy multiplier and trapped energy [1]. For RC-snubbers optimized so that minimal capacitance is used to achieve a certain overshoot ($\zeta=R/2\sqrt{(C/L)}$).

% Overshoot	ζ	X
5	2.1348	0.2404
10	1.4805	0.3554
20	1.0237	0.5404
30	0.8320	0.6994
40	0.7217	0.8486
50	0.6475	0.9933

In practice, soft voltage-clamps do not conduct current from Lseries at switch or diode turn-off instantaneously because of series clamp-inductance, and RC-snubbers are required across switch-diode pairs. Total passive snubbing energy eqn.4 is therefore increased by 2Wrc to give eqn.12 below.

$$Wtp=\frac{Vswitch}{di/dt}\frac{(Irm+Io)^2}{2}+Ls\frac{(Irm+Io^2)}{2} +2\left(1+\frac{2}{X^2}\right)Irm\ Lclamp$$

The BRT30P1-1000 data-sheet specifies Irm to vary according to (13). Irm of the BY103 is assumed to have a similar temperature dependency for fig.23.

$$Irm(Tj)=[0.64+4.8x10^{-3}(Tj-25)]Irm[100°C] \quad (13)$$

$$\Rightarrow Irm(Tj)=[0.64+4.8x10^{-3}(Tj-25)]Irm[25°C]/0.64 \quad (14)$$

REFERENCES

[1] F.V.P. Robinson and B.W. Williams, "Active or passive snubbing for fast switches?", Conf. Rec. IEEE Industrial Electronics Society Conference, Singapore, 1988, pp.617-622.

[2] C.C. Abbas, "Snubberless high-power rectifiers", Conf. Rec. Power Electronics Specialists Conference, 1986, pp.449-452.

[3] A.R. Hefner, "Analytical modelling of device -circuit interactions for the power insulated gate bipolar transistor (IGBT), Conf. Rec. IEEE Industry Applications Society Annual Meeting, 1988, pp.606-614.

[4] F.V.P. Robinson and B.W. Williams, "Accommodating parasitic effects in high-frequency power-stages", Conf. Rec. 3rd European Power Electronics and Applications Conf., Aachen, 1989.

[5] F.V.P. Robinson and B.W. Williams, "Optimising snubbers for high-current emitter-switched transistors", Conf. Rec. IEE Power Electronics and Variable Speed Drives Conference, London, 1988, pp.177-180.

[6] H.G. Skuderly et al, "A regenerative snubber for a 200 kVA GTO Inverter", Conf. Rec., IEEE Power Electronics Specialists Conf., Japan, 1988, pp.498-505.

[7] J.C. Bendien et al, "Recovery circuit for snubber energy in power electronic applications with high switching frequencies", IEEE Trans. on Power Electronics, Vol.3, No.1, 1988, pp.26-30.

[8] J. Kassakin and D. Lau, "An analysis and experimental verification of parasitic oscillation in paralleled power MOSFET's, IEEE Trans. Electron Devices, Vol. ED-31, No.7, July 1984, pp.959-963.

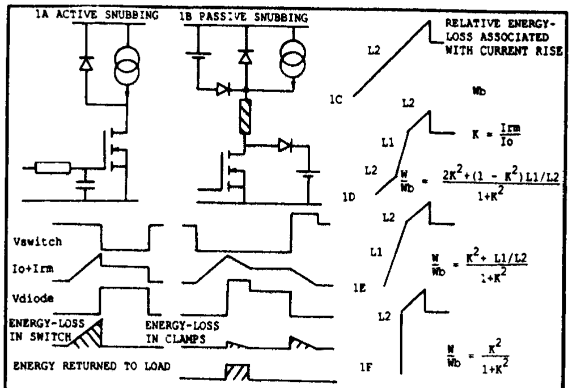


FIG.1 IDEALISED WAVEFORMS WITH ACTIVE AND PASSIVE SNUBBING

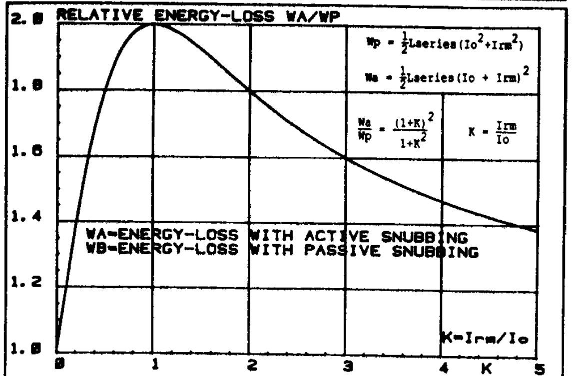


FIG.2 RELATIVE ENERGY-LOSS OF ACTIVE AND PASSIVE SNUBBING

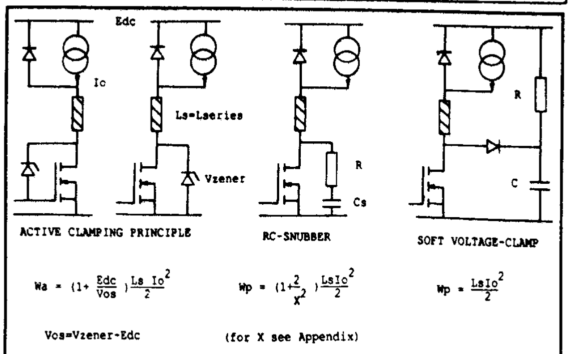
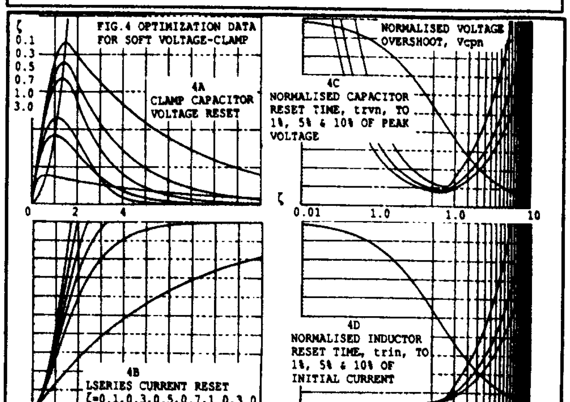
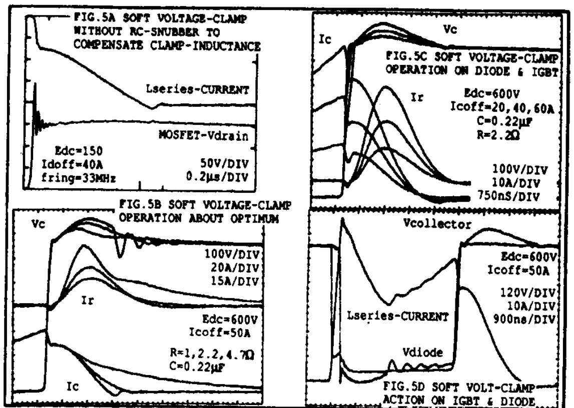


FIG.3 COMPARISON OF ACTIVE & PASSIVE TURN-OFF SNUBBER OR CLAMP EFFICIENCY





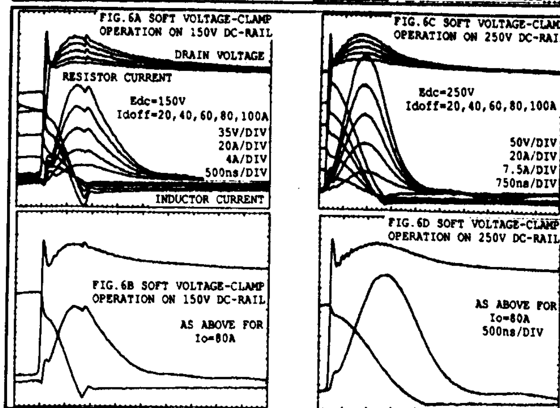
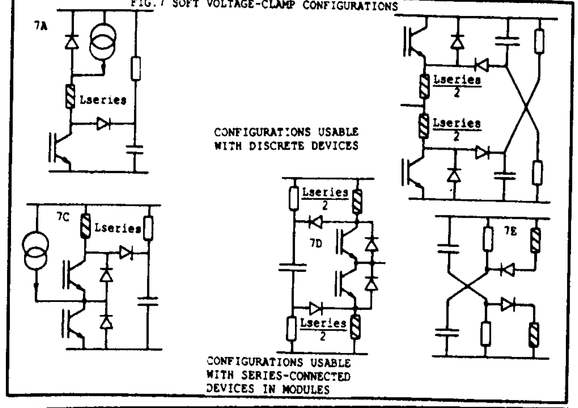
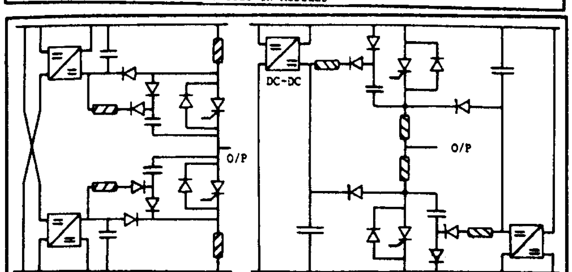


FIG.7 SOFT VOLTAGE-CLAMP CONFIGURATIONS

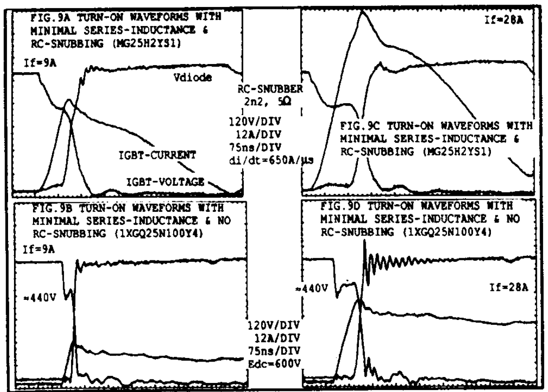


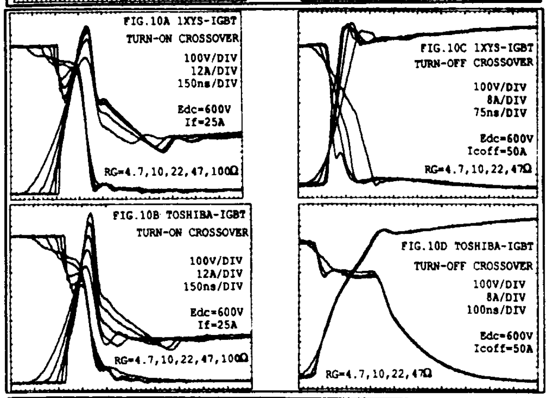


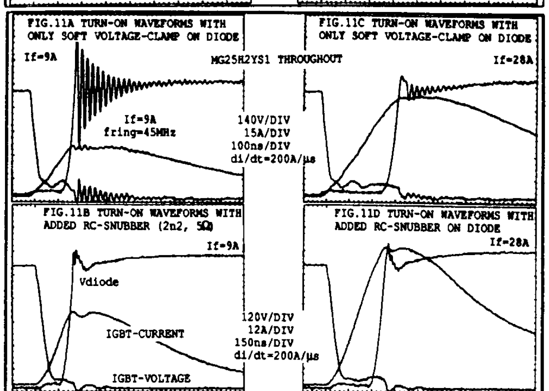
CONCENTRATED SERIES-SNUBBER INDUCTOR CLAMPED. STRAY-INDUCTANCE ENERGY PUT IN RCD-SNUBBER RATHER THAN VOLTAGE-CLAMPS

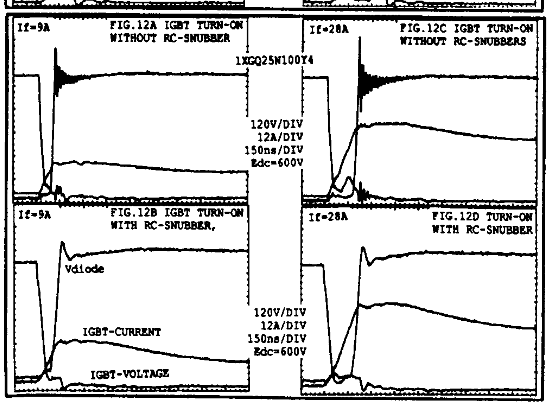
DEVICES DIRECTLY PROTECTED FROM dv/dt & OVERSHOOT. STRAY INDUCTANCE ACTS AS AS PART OF SERIES-SNUBBER INDUCTANCE

FIG.8 MODIFYING REGENERATIVE SNUBBER FOR IMPROVED CLAMPING









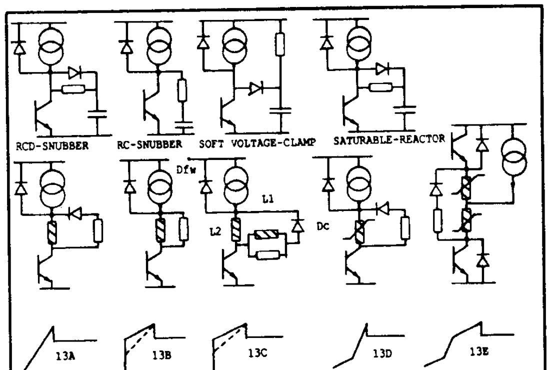


FIG.13 IDEALIZED CURRENT RISES FOR TURN-ON CURRENT DUALS OF VOLTAGE-SNUBBERS

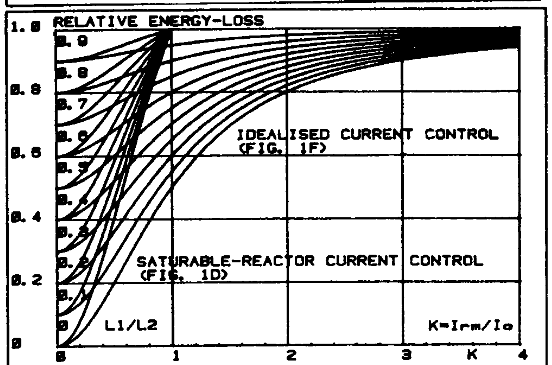


FIG.14 RELATIVE ENERGY-LOSS ASSOCIATED WITH FIG.1 CURRENT-RISES

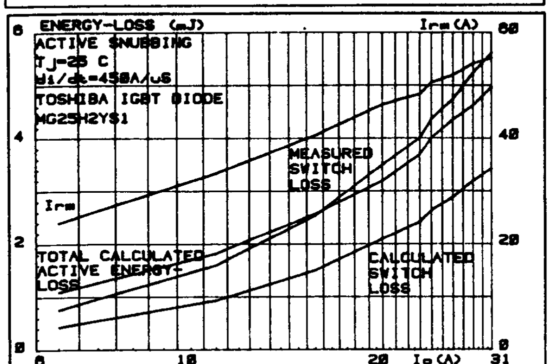


FIG.15 ACTIVE-SNUBBING ASSOCIATED ENERGY-LOSS VARIATION WITH CURRENT

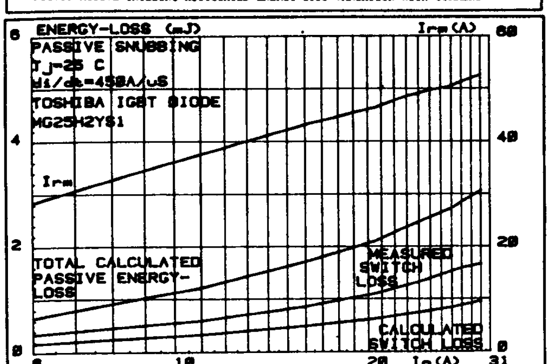


FIG.16 PASSIVE-SNUBBER ASSOCIATED ENERGY-LOSS VARIATION WITH CURRENT

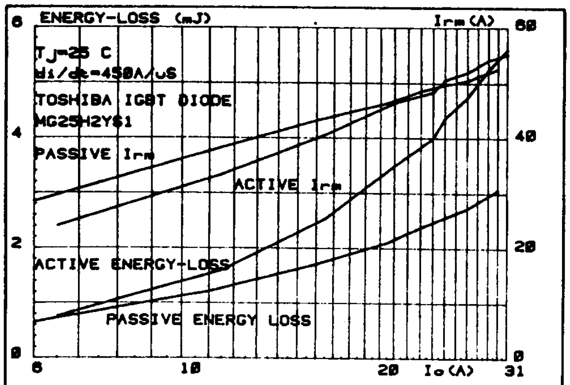


FIG.17 ACTIVE & PASSIVE SNUBBER ASSOCIATED ENERGY-LOSS FOR COMPARISON

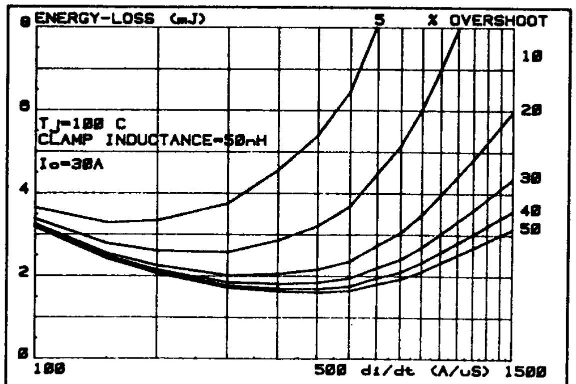


FIG.21 PASSIVE-SNUBBING ASSOCIATED LOSS VARIATION WITH TEMPERATURE

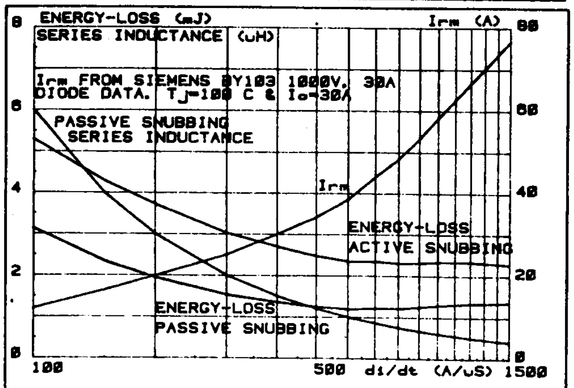


FIG.18 ACTIVE & PASSIVE SNUBBER ASSOCIATED ENERGY-LOSS VARIATION WITH di/dt

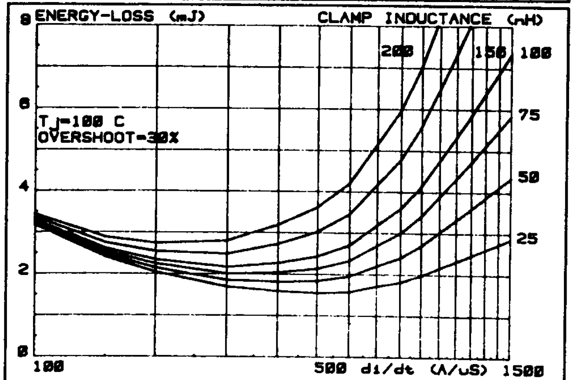


FIG.22 PASSIVE-SNUBBING ASSOCIATED LOSS VARIATION WITH CLAMP INDUCTANCE.

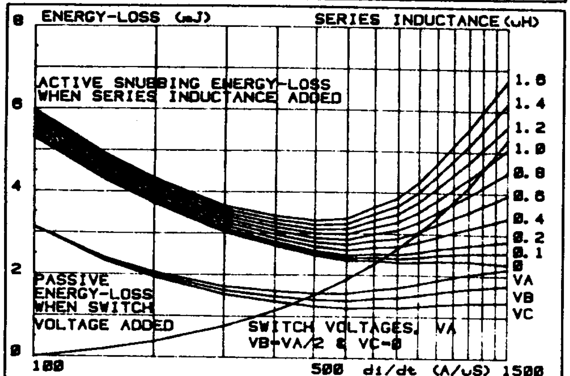


FIG.19 ACTIVE & PASSIVE ENERGY-LOSS ASSUMING Lseries≠0 & Vswitch≠0

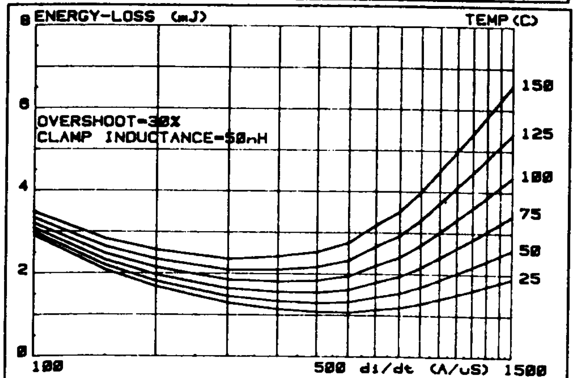


FIG.23 PASSIVE-SNUBBING ASSOCIATED LOSS VARIATION WITH RC-SNUBBER CAPACITY

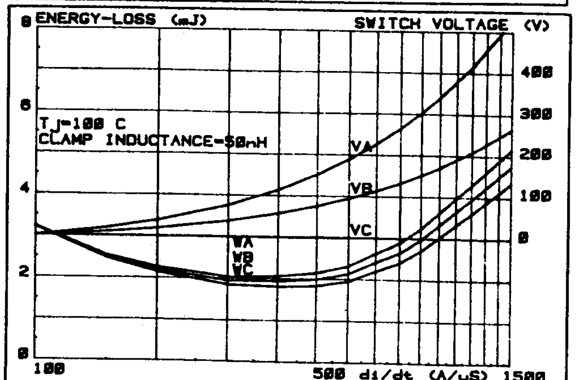


FIG.20 AFFECT OF Vswitch ON PASSIVE-SNUBBING LOSS WHEN RC-SNUBBER LOSS INCLUDED

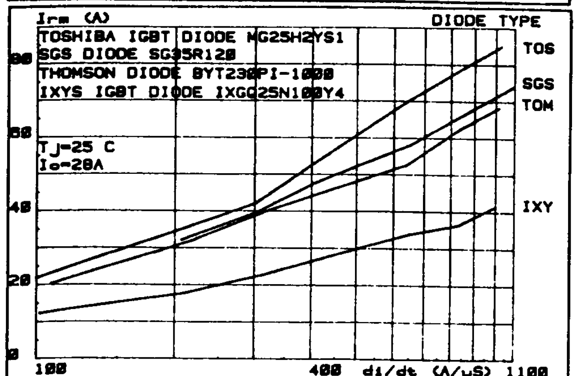


FIG.24 MEASURED Irm VALUES UNDER SAME CONDITIONS FOR 4 DIODE TYPES

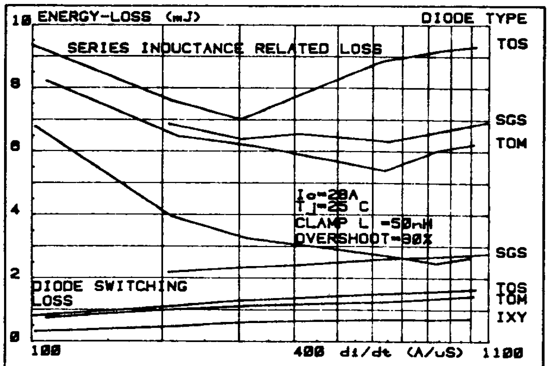


FIG.25 ENERGY-LOSS OF PASSIVE SNUBBING & MEASURED SWITCHING LOSS FOR 4 DIODES

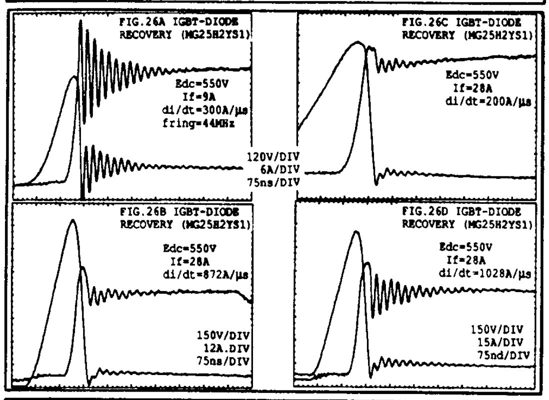


FIG.26A IGBT-DIODE RECOVERY (MG25H2YS1)

FIG.26B IGBT-DIODE RECOVERY (MG25H2YS1)

FIG.26C IGBT-DIODE RECOVERY (MG25H2YS1)

FIG.26D IGBT-DIODE RECOVERY (MG25H2YS1)

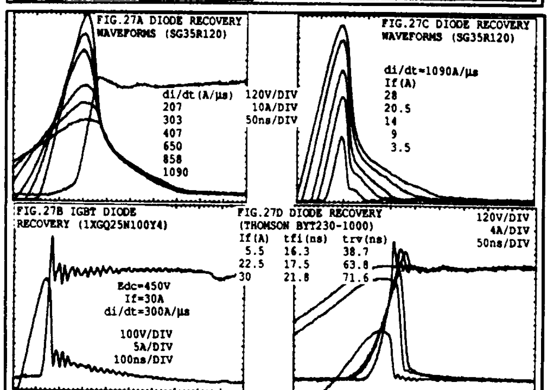


FIG.27A DIODE RECOVERY WAVEFORMS (SG35R120)

FIG.27B IGBT DIODE RECOVERY (1XGQ25N100Y4)

FIG.27C DIODE RECOVERY WAVEFORMS (SG35R120)

FIG.27D DIODE RECOVERY (THOMSON BYT230-1000)

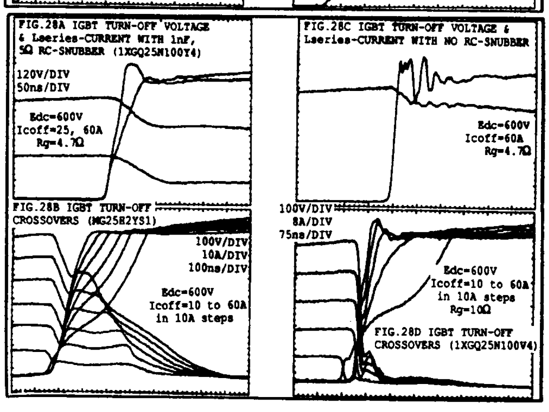


FIG.28A IGBT TURN-OFF VOLTAGE & Lseries-CURRENT WITH 1nF, 5Ω RC-SNUBBER (1XGQ25N100Y4)

FIG.28B IGBT TURN-OFF CROSSOVERS (MG25H2YS1)

FIG.28C IGBT TURN-OFF VOLTAGE & Lseries-CURRENT WITH NO RC-SNUBBER

FIG.28D IGBT TURN-OFF CROSSOVERS (1XGQ25N100Y4)

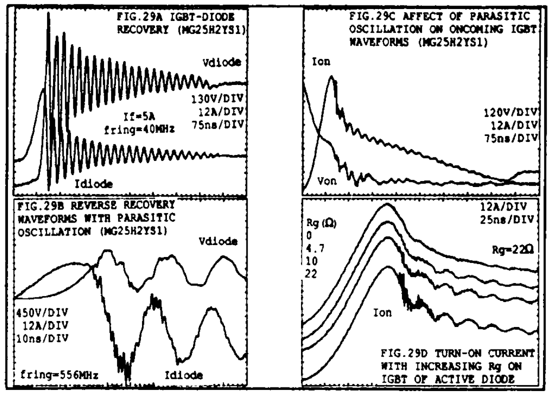


FIG.29A IGBT-DIODE RECOVERY (MG25H2YS1)

FIG.29B REVERSE RECOVERY WAVEFORMS WITH PARASITIC OSCILLATION (MG25H2YS1)

FIG.29C AFFECT OF PARASITIC OSCILLATION ON ONCOMING IGBT WAVEFORMS (MG25H2YS1)

FIG.29D TURN-ON CURRENT WITH INCREASING Rg ON IGBT OF ACTIVE DIODE

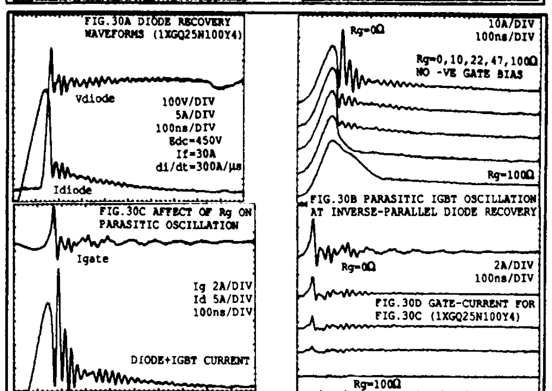


FIG.30A DIODE RECOVERY WAVEFORMS (1XGQ25N100Y4)

FIG.30B PARASITIC IGBT OSCILLATION AT INVERSE-PARALLEL DIODE RECOVERY

FIG.30C AFFECT OF Rg ON PARASITIC OSCILLATION

FIG.30D GATE-CURRENT FOR FIG.30C (1XGQ25N100Y4)

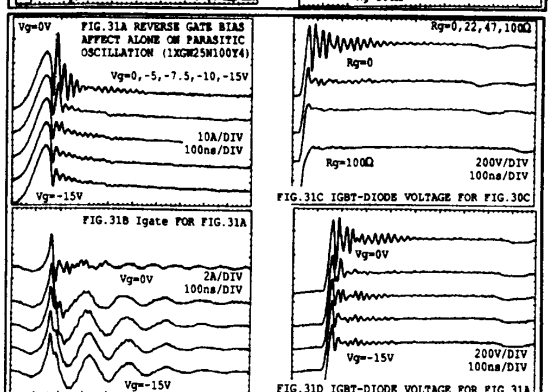


FIG.31A REVERSE GATE BIAS AFFECT ALONE ON PARASITIC OSCILLATION (1XGQ25N100Y4)

FIG.31B Igate FOR FIG.31A

FIG.31C IGBT-DIODE VOLTAGE FOR FIG.30C

FIG.31D IGBT-DIODE VOLTAGE FOR FIG.31A

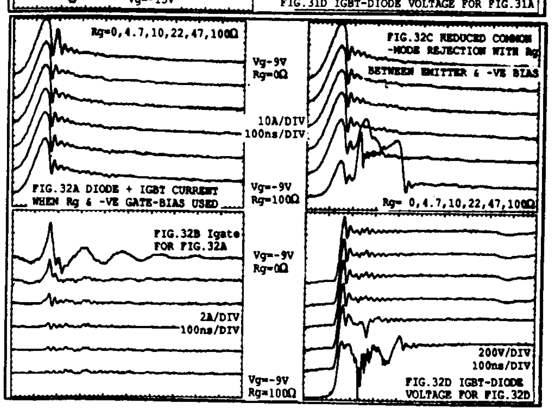


FIG.32A DIODE + IGBT CURRENT WHEN Rg & -VE GATE-BIAS USED

FIG.32B Igate FOR FIG.32A

FIG.32C REDUCED COMMON-MODE REJECTION WITH Rg BETWEEN EMITTER & -VE BIAS

FIG.32D IGBT-DIODE VOLTAGE FOR FIG.32D